# Distributed Shared Memory and Machine Learning

CSci 8211
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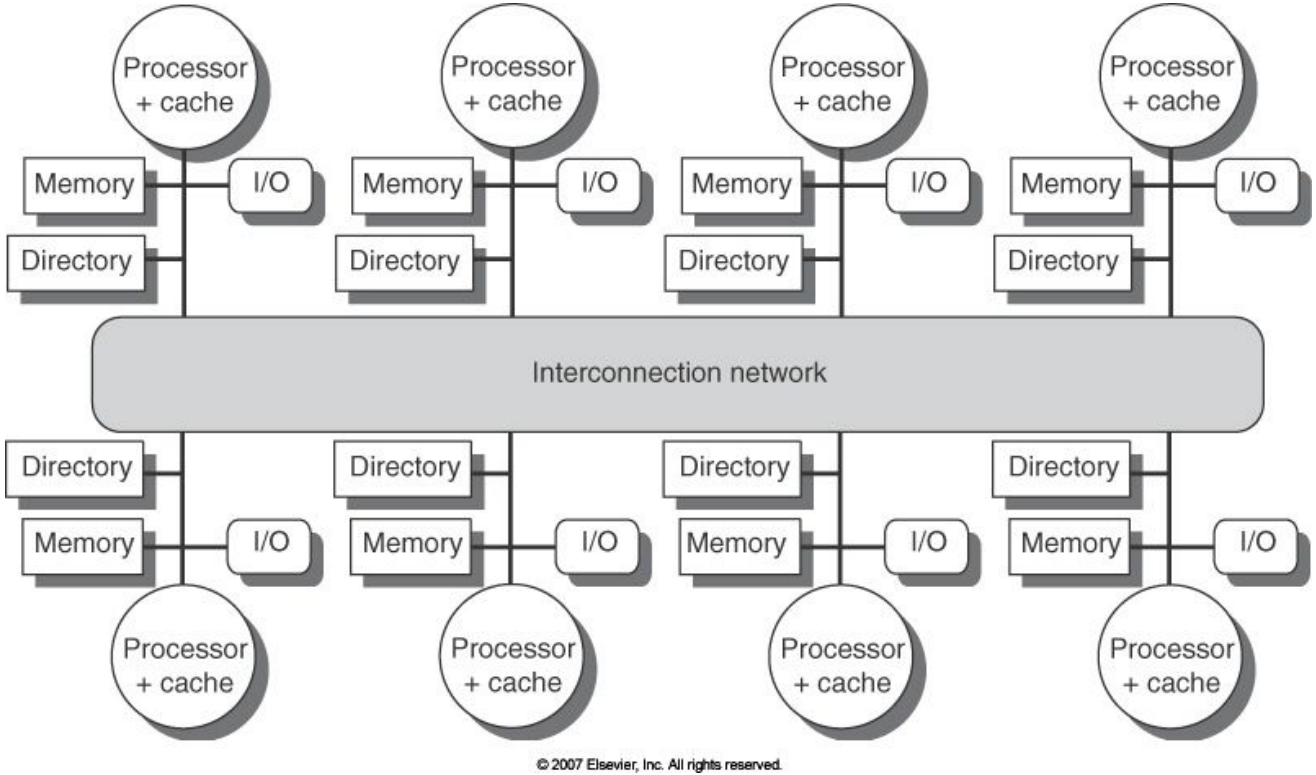
# Overview of Distributed Shared Memory (DSM)






Source: http://web.sfc.keio.ac.jp/~rdv/keio/sfc/teaching/architecture/architecture-2008/lec10-dsm.html

System performance:

- Lookup
- Action

# Key Issues

1. **DSM algorithm**
   - how accesses actually executes
2. **Implementation level**
   - where the access is implemented
3. **Memory consistency model**
   - how to maintain consistent

# DSM System Design Choices

- DSM algorithm
- Implementation level
- Memory consistency model
- Cluster configuration
- Interconnection network
- Structure of shared data
- Granualarity of shared data
- Data compression?

# DSM Systems and Algorithms

- **DSM systems** : all systems that provide shared memory abstraction on a distributed shared-memory system
- Basic problems:
  - **Distribution of shared data**
  - **Coherent view of shared data**

# DSM Systems and Algorithms

- Two strategies: *replication* and *migration*
- Algorithm classifications

| | | |
|---|---|---|
| SRSW | Single reader/single writer | No replication, maybe migration |
| MRSW | Multiple reader/single writer | Read replication, invalidation |
| MRMW | Multiple reader/multiple writer | Full replication |

# Implementation Level

| | | | |
|---|---|---|---|
| Software | User-level library, runtime system, OS kernel, language | 1-8 Kb | More flexible |
| Hardware | CC-NUMA<br>COMA<br>RMS | 4-128 bytes | Faster searching and directory functions |
| Hybrid | various | 16 bytes-8 Kb | Balance the cost-complexity trade-offs |

# Memory Consistency Model - The “trade-off”

- The legal ordering of memory references issued by a processor, as observed by other processors

| Memory consistency model | Strict | Loose |
|---|---|---|
| Memory consistency |  |  |
| Access latency |  |  |
| Bandwidth requirement |  |  |
| Programming simplicity |  |  |

# Memory Consistency Model - The “trade-off”

- Strong consistency models
  - *Sequential* consistency: the same sequence of reads and writes
  - *Processor* consistency: same sequence of writes
- More relaxed models
  - *Weak* consistency: consistent only on synchronization memory access
  - *Release* consistency: ordinary access between acquire/release pairs
  - *Lazy* release consistency: modifications wait until the next acquire
  - *Entry* consistency: use associated shared variable to protect protected shared variable

# What Can We Do -1

- How to do parallelization for a particular application?
  - Analyze its access pattern
  - Split the job into several sub-jobs
  - Parallel, not sequential
  - Independent
  - More reads, less writes

# What Can We Do -2

- Preprocessing the shared memory data
  - Predict next data migration/repetition in terms of
    - Usage
    - Size
    - Destination
  - Relocate/copy the data based on prediction

# What Can We Do -3

- Weigh between concurrency and consistency
  - Examine application before runtime for best consistency model
  - During runtime, change model accordingly
    - Memory miss
    - Bottleneck
    - Data source

# Papers


1. Jelica Protic (1996). **Distributed shared memory: Concepts and systems.** URL http://dx.doi.org/10.1109/88.494605
2. Tasoulas, Z.-G., Anagnostopoulos, I., Papadopoulos, L., & Soudris, D. (2018). **A Message-Passing Microcoded Synchronization for Distributed Shared Memory Architectures**. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *0070*(c), 1–1. https://doi.org/10.1109/TCAD.2018.2834423

# Papers

3. Vasava, H. D., Vasava, H. D., & Rathod, J. M. (2017). **Improving Performance of Distributed Shared Memory (DSM) on Multiprocessor Framework with Software Approach.** *Indian Journal of Science and Technology*, *10*(28), 1–7. https://doi.org/10.17485/ijst/2017/v10i28/112308

4. Nelson, J., Holt, B., Myers, B., Briggs, P., Ceze, L., Kahan, S., & Oskin, M. (2015). **Latency-Tolerant Software Distributed Shared Memory**. *Atc*, 291–305. Retrieved from https://www.usenix.org/conference/atc15/technical-session/presentation/nelson